REMARKS

Favorable consideration of this application in the view of the remarks to follow is respectfully requested. Since the present response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. § 1.116.

In order to expedite an allowance of Claims 1-10, applicants have cancelled the non-elected claims, i.e., Claims 11 – 40. The cancellation of these claims was done without prejudice or disclaimer.

In the outstanding Office Action, Claims 1-3, 5-8 and 10 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 6,586,311 to Wu ("Wu"). Claim 4 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Wu and U.S. Patent No. 6,777,752 to Osanai et al. ("Osanai et al."). Claim 9 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Wu and U.S. Patent No.5,554,873 to Erdeljac et al. ("Erdeljac et al.").

Concerning the § 102(b) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Wu since the applied reference does not disclose the claimed

structure recited in Claim 1. Specifically, Wu does not disclose a semiconductor IC structure comprising: a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof; at least one *metal resistor* located on, or in close proximity to, said surface of said semiconductor substrate, said at least one *metal resistor* comprising at least a conductive metal; and a first level of metallization above said at least one *metal resistor*. Applicants submit that the structure discussed in Wu is a *semiconductor resistor* formed within a semiconductor substrate below the top surface of the semiconductor substrate.

Wu does not disclose a metal resistor as indicated by the Examiner. The structure referred to by the Examiner in the outstanding Office Action as the metal resistor was indicated to be element 600. In accordance with Wu, element 600 is a silicide blocking structure (column 5 lines 57, 59, and 61; column 6 lines 4, 12, 21, 31, 37, 45, and 58 in Wu) which consists of an upper portion 550 (column 5 line 56, column 6 lines 4, 12 in Wu) and a lower portion 640 (column 6, lines 20 and 30 in Wu). This is also evident in FIGS. 5-8 in Wu.

Wu clearly recites that both the upper portion 550 and the lower portion 640 of element 60 are insulators. Column 5, lines 54-58 in Wu states "As shown in FIG. 5, the dielectric layer 450 may be patterned, using a photoresist mask (not shown), for example, to form an upper portion 550 of a silicide blocking structure 600, as shown in FIG. 6 and as described in more detail below." Therefore, the upper portion of the element 600 is made of a dielectric material since it is formed out of a dielectric layer. This point is confirmed by column 5, lines 39-40 in Wu, which states "As shown in FIG. 4, a dielectric layer 450 may be formed above the buffer layer 440." Another passage in column 51 lines 47-51 also reaffirms this point, which states "In one illustrative embodiment, the dielectric layer 450 is comprised of silicon nitride (Si_3N_4), having a thickness of ..." Therefore, ***the upper portion 550 of the silicide blocking element 600 in Wu is a dielectric layer and cannot be a metal or a metal silicide.***

The lower portion 640 of the silicide blocking structure 600 is also a dielectric layer. Column 6, lines 20-27 in Wu states that "As shown in FIG. 6, a lower portion 640 of the silicide blocking structure 600 may be formed by selectively patterning the buffer layer 440 (FIGS. 4 and 5), by an isotropic and/or an anisotropic etching technique, such as ..." Column 5, lines 22-30 in Wu states that "As shown in FIG. 4, a buffer layer 440 may be formed above the undoped polysilicon layer 430 and above the surface 405 of the structure layer 420. The buffer layer may be a nitride etch stop layer. The buffer layer 440 may be formed by a variety of known techniques for forming such layers, e.g., ..." Further varieties of the buffer layer 440 are described in column 5, lines 32-38 with the passage stating that "In one illustrative embodiment, the buffer layer 440 is comprised of either undoped oxide (UDOX), such as undoped silicon dioxide (SiO_2), or tetraethyl orthosilicate (TEOS), having a thickness of approximately 50A, formed by being blanket deposited by either a plasma enhanced PVD (PECVD) process or a low pressure CVD (LPCVD) process." Technically, TEOS is a precursor chemical for oxide deposition but often used as a misnomer for silicon dioxide formed with TEOS as a precursor chemical, as is the case in this passage. From these passages, it is clear the buffer layer 440 in Wu may be a nitride layer or an oxide layer. Both of them are dielectric materials. Since the lower portion 640 of the silicide blocking structure 600 is formed by selectively patterning the buffer layer 440, the lower portion 640 of the silicide blocking structure 600 is also a dielectric material. Therefore, ***the lower portion 640 of a silicide blocking structure 600 cannot be a metal or a metal silicide.***

Since none of the two components of the silicide blocking structure 600 are a metal or a metal silicide, the silicide blocking structure 600 cannot be a metal or a metal silicide. Furthermore, since both components of the silicide blocking structure 600 are actually dielectric

materials, it is impossible for the silicide blocking structure 600 to find an application as a resistor.

Wu provides a method of fabricating a semiconductor structure in which a salicide block mask prevents the formation of silicide on a portion of the silicon substrate. This is an improved method of forming a structure known prior to Wu. The resistor Wu's art refers to is a doped silicon resistor formed on the silicon substrate whereof Wu's art disclosed an improved method of manufacture. In accordance with Wu, the salicide block mask is located atop an undoped polysilicon region 430 that forms the resistor structure of the prior art. The resistor structure enabled by Wu is a prior art resistor located within the silicon substrate and ***comprises a doped silicon or undoped silicon.*** Wu's art does not enable either a metal resistor or a metal silicide resistor.

Applicants further note that Wu does not disclose a first metallization level atop the metal resistor, as presently claimed. A metallization level, as is well known to those skilled in the art, represents a dielectric material that has conductive features (conductive vias and/or lines) embedded therein. This is demonstrated in FIG. 3F in the present application. Therefore, ***metallization level must be able to pass significant amount of current for the operation of devices connected thereto.*** Applicants find no such metallization level in Wu. Applicants observe that the Examiner referred to element 700 as the alleged first metallization level. Applicants respectfully disagree regarding this interpretation of element 700. In Wu, element 700 is a blanket metal layer that is later used in forming a silicide contact. The metal layer 700 that is not consumed during the silicidation process is removed and thus does not form a first metallization level. This process is called salicidation (**Self Aligned silicidation**) in the semiconductor industry for the self aligning property, that is, no mask is used to pattern the silicide structure. In conventional semiconductor processing, the metal layer 700 is not patterned

lithographically on a dielectric surface to form a resistor structure made out of metal. There is no suggestion of patterning the metal layer 700 by lithographic means in Wu, either. Also, after the salicidation process, all unreacted material from the metal layer 700 is removed, therefore no elemental metal remains to form a metal resistor. Likewise, all the portions of the metal layer 700 that contact the silicon material react with the silicon and forms silicide. Any kind of structure formed out of the metal layer 700 is a contiguous silicide over polysilicon or the substrate. These do not meet the criteria for metallization on two counts. First, any structure that comes out of the metal layer 700 is actually a silicide structure, not a metal structure. Second, these structures do not form any vias or metal lines, as all normal metallization structures form, and the element 42 in FIG. 3F in the present application connotes. ***Therefore, structures obtained out of the metal layer 700 are not metallization, as it is referred to in the industry or in the present application.***

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosures of Wu. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the various obviousness rejections, applicants submit the combined disclosures of Wu and Osanai et al., or Erdeljac et al., do not render the claimed structures obvious since the applied reference does not teach or suggest the structure presently claimed. That is, the combined disclosures of Wu and Osanai et al., or Erdeljac et al., do not teach or suggest a semiconductor IC structure comprising: a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof; at least one *metal resistor* located on, or in close proximity to, said surface of said semiconductor substrate, said at least

one metal resistor comprising at least a conductive metal; and *a first level of metallization above said at least one metal resistor.*

The principal applied reference to Wu, which spurs each of the obviousness rejections, is defective for the reasons discussed above in regard to the anticipation rejection. Applicants thus incorporate the above remarks herein by reference. To reiterate: Wu discloses a salicide blocking structure comprising dielectric material. The only structure that may be used as resistors in Wu's art is the silicon within the substrate as doped or undoped silicon resistors, which would be a resistor made of semiconducting material. The applied reference does not teach or suggest a metal resistor, as presently claimed. Moreover, no metallization levels are taught or suggested in Wu.

The above defects in Wu are not alleviated by Osanai et al., and Erdeljak et. al., since the applied secondary references also do not teach or suggest the claimed structure in which a metal resistor is present and a first metallization level is located above the metal resistor. While Osanai et al., discloses metal resistor, it does not so in the context of including a first metallization level atop the metal resistor, as presently claimed. Erdeljak et al., is further removed that Osanai et al., since it is directed to polysilicon resistors, not metal resistors, as presently claimed.

In view of the above remarks, the obviousness rejections citing Wu and Osanai et al., or Erdeljak et al., have been obviated. Reconsideration and withdrawal of the obviousness rejections are thus respectfully requested.

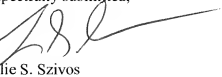
The various § 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed structures to include the various elements recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not

make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos
Registration No. 39,394

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza – Suite 300
Garden City, New York 11530
(516) 742-4343 (telephone)
(516) 742-4366 (facsimile)
LSS:BP:tam